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Linear CMOS RF Power Amplifiers for Wireless Applications Linear CMOS RF Power Amplifiers *RF CMOS Power Amplifiers: Theory, Design and Implementation* **CMOS RF Power Amplifier Design Approaches for Wireless Communications** *Reconfigurable CMOS RF Power Amplifiers for Advanced Mobile Terminals Transformer Array Power Combining and Stacking for CMOS RF Power Amplifiers Efficiency Enhancement Techniques for CMOS RF Power Amplifiers CMOS Radio-frequency Power Amplifiers for Multi-standard Wireless Communications* **CMOS RF Power Amplifiers for Mobile Wireless Communications High-Linearity CMOS RF Front-End Circuits Parasitic-aware Design and Optimization of CMOS RF Power Amplifier** RF Power Amplifiers for Mobile Communications CMOS RF Power Amplifier Design for Wireless Communications Efficient Linear CMOS RF Power Amplification **Design and Control of RF Power Amplifiers** *Class-A/D Approach for CMOS High Efficiency RF Power Amplifier* Wireless Ultra-Wideband Cmos Power Amplifiers *High Efficiency RF Power Amplifiers in CMOS for Low Power Wireless Communication Highly Efficient CMOS Power Amplifiers at C- and S-Band for Low Supply Voltages* **Optimized Class-E RF Power Amplifier Design in Bulk CMOS Design of an RF CMOS Power Amplifier for Wireless Sensor Networks Design of an RF Power Amplifier for Wireless Applications Using a CMOS Process RF Power Amplifier Using Deep Sub-micron CMOS Technology Analysis and Design of CMOS Transformer-based RF Power Amplifiers** Performance Limits of RF

Power CMOS **CMOS RF Transmitter Front-end Module for High-power Mobile Applications Digitally Enhanced CMOS RF Transmitter with Integrated Power Amplifier** Class-E Power Amplifiers and Transmitters for RF Applications **High Power CMOS RF Amplifier Module Expandable in Parallel** *Linearization and Efficiency Enhancement Techniques for Silicon Power Amplifiers* **RF and mm-Wave Power Generation in Silicon CMOS RF Tuned Power Amplifiers for Wireless Communications** *Radio Frequency Power Complementary Metal Oxide Semiconductors* **Design and Control of RF Power Amplifiers** Deeply Scaled CMOS for RF Power Applications *Millimeter-Wave Circuits for 5G and Radar* **CMOS Circuit Design for RF Sensors** *Switchmode RF Power Amplifiers* **Parasitic-Aware Optimization of CMOS RF Circuits** Silicon RF Power MOSFETS

This dissertation focuses on the design of CMOS power amplifiers for modern wireless handsets, where stringent linearity requirements and high power efficiency are difficult to achieve simultaneously. CMOS technology has been an attractive technology for research in fully-integrated transceivers due to its low cost and high-integration capability, as well as its continuously improving high-frequency performance. Its advantages, however, come at the cost of continuously reduced breakdown voltages, low isolation and high power loss in the substrate. To address these limitations, a stacked-FET design technique is first developed to systematically divide the voltage stress among several transistors connected in series, allowing the use of a larger supply voltage. The voltage swing of each stacked device is added in phase to provide a larger output power to the load without the requirement of a large impedance transformation. To investigate this technique, a fully-integrated 20 dBm RF power amplifier is first implemented using 0.25-[mu]m silicon-on-sapphire MOSFETs. By using triple-stacked FETs, the optimum load impedance for a 20 dBm power amplifier increases to 50 [Omega] so impedance transformation is not required at the output. Measurement of a single-stage linear power amplifier shows a small-signal gain of 17.1 dB and a saturated output power of 21.0 dBm with a power added efficiency (PAE) of 44.0% at 1.88 GHz. With an IS-95 code division multiple access (CDMA) modulated signal, the power amplifier shows average output power of 16.3 dBm and PAE of 18.7% with ACPR below -42 dBc. The concept is then further demonstrated at higher voltage and power level. A single-stage quadruple-stacked-FET linear power amplifier is presented using 0.28-[mu]m 2.5-V standard I/O FETs in a 0.13- & mu;m silicon-on-insulator (SOI) CMOS technology. The PA is designed to withstand up to 9 V of supply voltage before reaching its breakdown limit. The measured PA achieves a small-signal gain of 14.6 dB, a saturated output

power of 32.4 dBm, and a PAE of 47% at 1.9 GHz with a 6.5-V supply. Using a reverse-link IS-95 CDMA modulated signal, the PA shows an average output power of up to 28.7 dBm with a PAE of 41.2% while meeting the adjacent channel power ratio requirement. The PA also shows an average output power of up to 29.4 dBm with a PAE of 41.4% while meeting the adjacent channel leakage ratio requirement of an uplink wideband code division multiple access (WCDMA) modulated signal. These performances are comparable to those of GaAs-based power amplifiers. To fully exploit the advantages of higher-speed CMOS technology and the availability of co-integrated digital circuitry, a digital-intensive transceiver architecture is explored as an alternative in the second part of the dissertation. A single-ended digitally-modulated power amplifier (DPA) is demonstrated in a 0.13-[mu]m 1.2-V SOI CMOS technology, to be used in a multi-standard RF polar transmitter. The amplitude modulation is done by digitally controlling the number of activated unit amplifiers whose currents are summed at the output. The DPA is designed for multi-mode multi-band functionality by avoiding frequency-selective components, except for the final-stage output matching network. The measured DPA delivers a 24.9-dBm peak output power at 900 MHz with a maximum power efficiency of 62.7%. Similar high-efficiency performance is also exhibited at 1.92 GHz with a reconfigured matching network. By employing a digital pre-distortion technique, the DPA could meet linearity requirements for both the enhanced data rate for GSM evolution (EDGE) and WCDMA standards. This book provides an overview of current efficiency enhancement and linearization techniques for silicon power amplifier designs. It examines the latest state of the art technologies and design techniques to address challenges for RF cellular mobile, base stations, and RF and mmW WLAN applications. Coverage includes material on current silicon (CMOS, SiGe) RF and mmW power amplifier designs, focusing on advantages and disadvantages compared with traditional GaAs implementations. With this book you will learn: The principles of linearization and efficiency improvement techniques The architectures allowing the optimum design of multimode Si RF and mmW power amplifiers How to make designs more efficient by employing new design techniques such as linearization and efficiency improvement Layout considerations Examples of schematic, layout, simulation and measurement results Addresses the problems of high power generation, faithful construction of non-constant envelope constellations, and efficient and well control power radiation from integrated silicon chips Demonstrates how silicon technology can solve problems and trade-offs of power amplifier design, including price, size, complexity and efficiency Written and edited by the top contributors to the field This book tackles both high efficiency and high linearity power amplifier (PA) design in low-voltage CMOS. With its emphasis on theory, design and

implementation, the book offers a guide for those actively involved in the design of fully integrated CMOS wireless transceivers. Offering mathematical background, as well as intuitive insight, the book is essential reading for RF design engineers and researchers and is also suitable as a text book. The telecommunication market calls for the integration of complicated wireless applications. To build RF power amplifiers in CMOS remains challenging due to the non-ideal effects in CMOS. The aim of this thesis is to provide an optimized yet explicit design method for the Class-E amplifiers in CMOS. Taking the finite DC feed inductor into consideration, a simple but accurate numerical design method is proposed by applying polynomial interpolation. Combining with a practical design strategy for non-ideal transistors of finite conductance and parasitic capacitances, a two-staged Class-E power amplifier is implemented in 0.18mum CMOS. The simulation results show that this power amplifier can deliver at least a 23dBm power to a 50Ohm load with 73.5% PAE at 2.4GHz. The good agreement between simulation results and the predicted values validates this design method and its applications in CMOS. This method could be applied to general design cases. The work establishes the design flow for the optimization of linear CMOS power amplifiers from the first steps of the design to the final IC implementation and tests. The authors also focuses on design guidelines of the inductor’s geometrical characteristics for power applications and covers their measurement and characterization. Additionally, a model is proposed which would facilitate designs in terms of transistor sizing, required inductor quality factors or minimum supply voltage. The model considers limitations that CMOS processes can impose on implementation. The book also provides different techniques and architectures that allow for optimization. "This thesis presents the design process of a class E RF power amplifier and a transmitter in a standard CMOS technology. CMOS radio frequency class-E power amplifiers (PA) for GMSK/GFSK modulations have been designed and fabricated using 0.25/0.35mum technologies. The operating frequencies are centered at 1.2GHz and 2.65GHz with 24--26dBm output power. In order to reduce the driving requirement, mode locking techniques are employed for both designs. High efficiency broadband off-chip hybrid ring baluns are used at both input and output for converting signals from single-ended to differential and vice versa. Regular bonding wires are used as inductors for the 1.2GHz PA, and on-chip bondwires are used for the 2.65GHz PA. With a 1.3V supply, the measured power added efficiency (PAE) of the 1.2GHz PA, after taking into account the losses in the baluns, is 62%. The PAE for the 2.65GHz PA is 38% when operated from a 1.7V power supply. Furthermore, a transmitter stage for 5.5GHz frequency application has been designed and simulated using a 0.18mum CMOS technology. The design and layout is completed, with a simulation frequency of 5.9GHz and an output signal of 7dBm." --

Design and Control of RF Power Amplifiers investigates various architectures and concepts for the design and control of radio-frequency (RF) power amplifiers. This book covers merits and challenges of integrating RF power amplifiers in various technologies, and introduces a number of RF power amplifier performance metrics. It provides a thorough review of various power amplifier topologies, followed by a description of approaches and architectures for the control and linearization of these amplifiers. A novel parallel amplifier architecture introduced in this book offers a breakthrough solution to enhancing efficiency in systems using power control. Design and Control of RF Power Amplifiers is a valuable resource for designers, researchers and students in the field of RF integrated circuit design. Detailed and thorough coverage of various concepts in RF power amplifier design makes this book an invaluable guide for both beginners and professionals. This book focuses on high performance radio frequency integrated circuits (RF IC) design in CMOS. 1. Development of radio frequency ICs Wireless communications has been advancing rapidly in the past two decades. Many high performance systems have been developed, such as cellular systems (AMPS, GSM, TDMA, CDMA, W-CDMA, etc.), GPS system (global po- tioning system) and WLAN (wireless local area network) systems. The rapid growth of VLSI technology in both digital circuits and analog circuits provides benefits for wireless communication systems. Twenty years ago not many p- ple could imagine millions of transistors in a single chip or a complete radio for size of a penny. Now not only complete radios have been put in a single chip, but also more and more functions have been realized by a single chip and at a much lower price. A radio transmits and receives electro-magnetic signals through the air. The signals are usually transmitted on high frequency carriers. For example, a t- ical voice signal requires only 30 Kilohertz bandwidth. When it is transmitted by a FM radio station, it is often carried by a frequency in the range of tens of megahertz to hundreds of megahertz. Usually a radio is categorized by its carrier frequency, such as 900 MHz radio or 5 GHz radio. In general, the higher the carrier frequency, the better the directivity, but the more difficult the radio design. RF CMOS Power Amplifiers: Theory Design and Implementation focuses on the design procedure and the testing issues of CMOS RF power amplifiers. This is the first monograph addressing RF CMOS power amplifier design for emerging wireless standards. The focus on power amplifiers for short is distance wireless personal and local area networks (PAN and LAN), however the design techniques are also applicable to emerging wide area networks (WAN) infrastructure using micro or pico cell networks. The book discusses CMOS power amplifier design principles and theory and describes the architectures and tardeoffs in designing linear and nonlinear power amplifiers. It then details design examples of RF CMOS power amplifiers for short distance wireless

applications (e, g., Bluetooth, WLAN) including designs for multi-standard platforms. Design aspects of RF circuits in deep submicron CMOS are also discussed. RF CMOS Power Amplifiers: Theory Design and Implementation serves as a reference for RF IC design engineers and RD and R&D managers in industry, and for graduate students conducting research in wireless semiconductor IC design in general and with CMOS technology in particular. Design and Control of RF Power Amplifiers investigates various architectures and concepts for the design and control of radio-frequency (RF) power amplifiers. This book covers merits and challenges of integrating RF power amplifiers in various technologies, and introduces a number of RF power amplifier performance metrics. It provides a thorough review of various power amplifier topologies, followed by a description of approaches and architectures for the control and linearization of these amplifiers. A novel parallel amplifier architecture introduced in this book offers a breakthrough solution to enhancing efficiency in systems using power control. Design and Control of RF Power Amplifiers is a valuable resource for designers, researchers and students in the field of RF integrated circuit design. Detailed and thorough coverage of various concepts in RF power amplifier design makes this book an invaluable guide for both beginners and professionals. (Cont.) However, since I/O devices are often included as part of the process, they represent a real option for PA integration because they allow for higher power densities. The 0.25 /xm I/O device that is available in the 90 nm process, when biased at Vdd = 2.5 V showed excellent results, with a peak PAE of 60% and an output power of 75 mW (125 mW/mm) at 8 GHz. In recent years, tremendous growth of the wireless market can be defined through the following words: smartphone and high-data rate wireless communication. This situation gives new challenges to RF power amplifier design, which includes high-efficiency, multi-band operation, and robustness to antenna mismatch conditions. In addition to these issues, the industry and consumers demand a low-cost small-sized wireless device. A fully integrated single-chip CMOS transceiver is the best solution in terms of cost and level of integration with other functional blocks. Therefore, the effective approaches in a CMOS process for the abovementioned hurdles are highly desirable. In this dissertation, the new challenges are overcome by introducing adaptability to a CMOS power amplifier. Meaningful achievements are summarized as follows. First, a new CMOS switched capacitor structure for high power applications is proposed. Second, a dual-mode CMOS PA with an integrated tunable matching network is proposed to extend battery lifetime. Third, a switchless dual-band matching structure is proposed, and the effectiveness of dual-band matching is demonstrated with a fully-integrated CMOS PA. Lastly, a reconfigurable CMOS PA with an automatic antenna mismatch recovery system is presented, which can maintain its original designed performance

even under various antenna mismatch conditions. Conclusively, the research in this dissertation provides various solutions for new challenges of advanced mobile terminals. Advances in electronics have pushed mankind to create devices, ranging from - credible gadgets to medical equipment to spacecraft instruments. More than that, modern society is getting used to—if not dependent on—the comfort, solutions, and astonishing amount of information brought by these devices. One ?eld that has continuously bene?tted from those advances is the radio frequency integrated c- cuit (RFIC) design, which in its turn has promoted countless bene?ts to the mankind as a payback. Wireless communications is one prominent example of what the - vances in electronics have enabled and their consequences to our daily life. How could anyone back in the eighties think of the possibilities opened by the wireless local area networks (WLANs) that can be found today in a host of places, such as public libraries, coffee shops, trains, to name just a few? How can a youngster, who lives this true WLAN experience nowadays, imagine a world without it? This book dealswith the design oflinearCMOS RF PowerAmpli?ers(PAs). The RF PA is a very important part of the RF transceiver, the device that enables wireless communications. Two important aspects that are key to keep the advances in RF PA design at an accelerate pace are treated: ef?ciency enhancement and frequen- tunable capability. For this purpose, the design of two different integrated circuits realizedina0. 11?mtechnologyispresented,eachoneaddressingadifferentaspect. With respect to ef?ciency enhancement, the design of a dynamic supply RF power ampli?er is treated, making up the material of Chaps. 2 to 4. "The world-wide proliferation of cellular networks has revolutionized telecommunication systems. The transition from Analog to Digital RF technology enabled substantial increase in voice traffic using available spectrum, and subsequently the delivery of digitally based text messaging, graphics and even streaming video. The deployment of digital networks has required migration to multi-carrier RF power amplifiers with stringent demands on linearity and efficiency. This book describes the physics, design considerations and RF performance of silicon power Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs) that are at the heart of the power amplifiers. The recent invention and commercialization of RF power MOSFETs based on the super-linear mode of operation is described in this book for the first time. In addition to the analytical treatment of the physics, extensive description of transistor operation is provided by using the results of numerical simulations. Many novel power MOSFET structures are analyzed and their performance is compared with those of the laterally-diffused (LD) MOSFET that are currently used in 2G and 3G networks."--BOOK JACKET.Title Summary field provided by Blackwell North America, Inc. All Rights Reserved The development of multi-standard wireless communication systems with low cost

and high integration is continuously requested and accompanied by the explosive growth of the wireless communication market. Although CMOS technology can provide most building blocks in RF transceivers, the implementation of CMOS RF power amplifiers is still a challenging task. The objective of this research is to develop design techniques to implement fully-integrated multi-mode power amplifiers using CMOS technology. In this dissertation, a load modulation technique with tunable matching networks and a pre-distortion technique in a multi-stage PA are proposed to support multi-communication standards with a single PA. A fully-integrated dual-mode GSM/EDGE PA was designed and implemented in a 0.18 um CMOS technology to achieve high output power for the GSM application and high linearity for the EDGE application. With the suggested power amplifier design techniques, fully-integrated PAs have been successfully demonstrated in GSM and EDGE applications. In Addition to the proposed techniques, a body-switched cascode PA core is also proposed to utilize a single PA in multi-mode applications without hurting the performance. With the proposed techniques, a fully-integrated multi-mode PA has been implemented in a 0.18 um CMOS technology, and the power amplifier has been demonstrated successfully for GSM/EDGE/WCDMA applications. In conclusion, the research in this dissertation provides CMOS RF power amplifier solutions for multiple standards in mobile wireless communications with low cost and high integration. CMOS technology scaling has enabled the integration of RF transceivers on a single chip for various applications. However, as the feature sizes of the transistors scale, their breakdown voltages are reduced. Lower breakdown voltages lower the maximum voltage swings across the transistors and necessitate operation from a lower supply voltage. These factors, in turn, impose significant limitations on RF power amplifier design: (1) the low voltage swings limit the maximum power that can be delivered to the load, and (2) the DC-DC converter needed to generate a low supply voltage for the power amplifier from typical battery voltages increases the power consumption, size, and cost of the design. To address the first challenge, transistor stacking and transformer-based power combining are investigated as means of increasing the output power, while to address the second issue, transistor stacking and amplifier stacking are considered. Two CMOS RF power amplifier architectures serve as vehicles for exploring these concepts, each leading to the design and implementation of an experimental prototype. The first design is based on a stacked amplifier architecture with an off-chip matching network. Transistor stacking is used to increase the output power and supply voltage of the power amplifier, and a bias circuit is designed to enable operation of the power amplifier from a large supply voltage without exceeding the transistor breakdown limitations. The second design is an array RF PA architecture that employs (1) series-parallel transformers, (2) transistor

stacking, and (3) amplifier stacking. This array RF PA uses series-parallel combinations of transformers to provide simultaneous impedance transformation and power combining. The proposed scalable transformer array architecture offers the possibility of designing a power amplifier to meet given specifications of output power and load impedance over a wide bandwidth. Stacking transistors in the array RF PA increases the output power provided by each of the unit PA stages comprising the array. In addition, the PA stages are themselves stacked. The two stacking methods increase the operating supply voltage. To demonstrate the proposed concept, a 2-by-4 amplifier array has been integrated in a 65-nm CMOS technology. This book presents the challenges and solutions of designing power amplifiers at RF and mm-Wave frequencies in a silicon-based process technology. It covers practical power amplifier design methodologies, energy- and spectrum-efficient power amplifier design examples in the RF frequency for cellular and wireless connectivity applications, and power amplifier and power generation designs for enabling new communication and sensing applications in the mm-Wave and THz frequencies. With this book you will learn: Power amplifier design fundamentals and methodologies Latest advances in silicon-based RF power amplifier architectures and designs and their integration in wireless communication systems State-of-the-art mm-Wave/THz power amplifier and power generation circuits and systems in silicon Extensive coverage from fundamentals to advanced design topics, focusing on various layers of abstraction: from device modeling and circuit design strategy to advanced digital and mixed-signal architectures for highly efficient and linear power amplifiers New architectures for power amplifiers in the cellar and wireless connectivity covering detailed design methodologies and state-of-the-art performances Detailed design techniques, trade-off analysis and design examples for efficiency enhancement at power back-off and linear amplification for spectrally-efficient non-constant envelope modulations Extensive coverage of mm-Wave power-generation techniques from the early days of the 60 GHz research to current state-of the-art reconfigurable, digital mm-Wave PA architectures Detailed analysis of power generation challenges in the higher mm-Wave and THz frequencies and novel technical solutions for a wide range for potential applications, including ultrafast wireless communication to sensing, imaging and spectroscopy Contributions from the world-class experts from both academia and industry This useful reference is about CMOS circuit design for sensor and actuators to be used in wireless RF systems. It places special focus on the power and data link in a wireless system with transducers powered via the RF link, presenting novel principles and methods. With the explosive growth of the wireless market, the demand for low-cost and highly-integrated radio frequency (RF) transceiver has been increased. Keeping up with this trend, complimentary metal-oxide-semiconductor (CMOS) has

been spotlighted by virtue of its superior characteristics. However, there are challenges in achieving this goal, especially designing the transmitter portion. The objective of this research is to demonstrate the feasibility of fully integrated CMOS transmitter module which includes power amplifier (PA) and transmit/receive (T/R) switch by compensating for the intrinsic drawbacks of CMOS technology. As an effort to overcome the challenges, the high-power handling T/R switches are introduced as the first part of this dissertation. The proposed differential switch topology and feed-forward capacitor helps reducing the voltage stress over the switch devices, enabling a linear power transmission. With the high-power T/R switches, a new transmitter front-end topology - differential PA and T/R switch topology with the multi-section PA output matching network - is also proposed. The multi-stage PA output matching network assists to relieve the voltage stress over the switch device even more, by providing a low switch operating impedance. By analyzing the power performance and efficiency of entire transmitter module, design methodology for the high-power handling and efficient transmitter module is established. Finally, the research in this dissertation provides low-cost, high-power handling, and efficient CMOS RF transmitter module for wireless applications. A majority of people now have a digital mobile device whether it be a cell phone, laptop, or blackberry. Now that we have the mobility we want it to be more versatile and dependable; RF power amplifiers accomplish just that. These amplifiers take a small input and make it stronger and larger creating a wider area of use with a more robust signal. Switching mode RF amplifiers have been theoretically possible for decades, but were largely impractical because they distort analog signals until they are unrecognizable. However, distortion is not an issue with digital signals—like those used by WLANs and digital cell phones—and switching mode RF amplifiers have become a hot area of RF/wireless design. This book explores both the theory behind switching mode RF amplifiers and design techniques for them. *Provides essential design and implementation techniques for use in cma2000, WiMAX, and other digital mobile standards *Both authors have written several articles on the topic and are well known in the industry *Includes specific design equations to greatly simplify the design of switchmode amplifiers The Power Amplifier (PA) is the last Radio Frequency (RF) building block in a transmitter, directly driving an antenna. The low power RF input signal of the PA is amplified to a significant power RF output signal by converting DC power into RF power. Since the PA consumes a majority of the power, efficiency plays one of the most important roles in a PA design. Designing an efficient, fully integrated RF PA that can operate at low supply voltage (1.2V), low power, and low RF frequency (433MHz) is a major challenge. The class E Power Amplifier, which is one type of switch mode PA, is preferred in such a scenario because of its higher theoretical efficiency compared to linear

power amplifiers. A controllable class E RF power amplifier design implemented in 0.13 microm CMOS process is presented. The circuit was designed, simulated, laid out, fabricated, and tested. The PA will be integrated as a part of a complete wireless transceiver system using the same process WIRELESS ULTRA-WIDEBAND CMOS POWER AMPLIFIERS: Design and Implementation focus on the theory, design, fabrication and testing of CMOS RF power amplifiers. This book has addressed the state-of-the-art and the latest achievements in CMOS technology UWB power amplifiers design. It has taken a theoretical and experimental approach to some extent, which is more useful to the reader. The book highlights the unique design issues which put the reader in good pace to be able to understand more advanced research. This book covers the background and fundamental theory of power amplifiers, the class of operation, the performance criteria and power amplifier circuits design and implementation in CMOS technology. Read this book to learn more about the design techniques for realizing wide bandwidth power amplifiers for UWB applications. It then details design example of wideband CMOS power amplifiers. This book is a comprehensive reference to students as well as practicing professionals in academia and industry working in the areas of power amplifier circuits design as well as in transmitter wireless device development. Wireless and mobile communication systems have become ubiquitous in our daily life. The need for higher bandwidth and thus higher speed and data rates in wireless communications has prompted the exploration of millimeter-wave frequencies. Some of the applications in this regime include high-speed wireless local area networks and high data rate personal area networks at 60 GHz, automotive collision avoidance radar at 77 GHz and millimeter-wave imaging at 94 GHz. Most of these applications are cost sensitive and require high levels of integration to reduce system size. The tremendous improvement in the frequency response of state-of-the-art deeply scaled CMOS technologies has made them an ideal candidate for millimeter-wave applications. A few research groups have already demonstrated single chip CMOS radios at 60 GHz. However, the design of power amplifiers in CMOS still remains a significant challenge because of the low breakdown voltage of deep submicron CMOS technologies. Power levels from 60 GHz power amplifiers have been limited to around 15 dBm with power-added efficiencies in the 10-20% range, despite the use of multiple gain stages and power combining techniques. In this work, we have studied the RF power potential of commercial 65 nm and 45 nm CMOS technologies. We have mapped the frequency, power and efficiency limitations of these technologies and identified the physical mechanisms responsible for these limitations. We also present a simple analytical model that allows circuit designers to estimate the maximum power obtainable from their designs for a given efficiency. The model uses only the DC

bias point and on-resistance of the device as inputs and contains no adjustable parameters. We have demonstrated a record output power density of 210 mW/mm and power-added efficiency in excess of 75% at VDs = 1.1 V and f = 2 GHz on 45 nm CMOS devices. This record power performance was made possible through careful device layout for minimized parasitic resistances and capacitances. Total output power approaching 70 mW was measured on 45 nm CMOS devices by increasing the device width to 640 gm. However, we find that the output power scales non-ideally with device width because of an increase in normalized on-resistance in the wide devices. PAE also decreases with increasing device width because of degradation in f. in the wide devices. Additionally PAE decreases as the measurement frequency increases, though the output power remains constant with increasing frequency. Small-signal equivalent circuit extractions on these devices suggest that the main reason for the degradation in the normalized output power and PAE with increasing device width is the non-ideal scaling of parasitic gate and drain resistances in the wide devices. In the arena of parasitic-aware design of CMOS RF circuits, efforts are aimed at the realization of true single-chip radios with few, if any, off-chip components. The parasitic-aware RF circuit synthesis techniques described in this book effectively address critical problems in this field. The advent of high-bandwidth, highly spectral-efficient communication protocols, such as IEEE 802.11g, has imposed tremendous challenges on RF power amplifier design. Since the power amplifier is often the most power-consuming block in a wireless system, its efficiency can have a determining impact on the battery life of the system. However, the high linearity required in many current and emerging wireless systems has typically mandated the use of highly linear traditional class-A designs that have a relatively low efficiency. Discover the concepts, architectures, components, tools, and techniques needed to design millimeter-wave circuits for current and emerging wireless system applications. Focusing on applications in 5G, connectivity, radar, and more, leading experts in radio frequency integrated circuit (RFIC) design provide a comprehensive treatment of cutting-edge physical-layer technologies for radio frequency (RF) transceivers - specifically RF, analog, mixed-signal, and digital circuits and architectures. The full design chain is covered, from system design requirements through to building blocks, transceivers, and process technology. Gain insight into the key novelties of 5G through authoritative chapters on massive MIMO and phased arrays, and learn about the very latest technology developments, such as FinFET logic process technology for RF and millimeter-wave applications. This is an essential reading and an excellent reference for high-frequency circuit designers in both academia and industry.

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- Radio Frequency Power Complementary Metal Oxide Semiconductors
- Design And Control Of RF Power Amplifiers
- Deeply Scaled CMOS For RF Power Applications
- Millimeter Wave Circuits For 5G And Radar
- CMOS Circuit Design For RF Sensors
- Switchmode RF Power Amplifiers
- Parasitic Aware Optimization Of CMOS RF Circuits
- Silicon RF Power MOSFETS