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Topics International Directory of Company Histories Plunkett's InfoTech Industry Almanac Architecture Design and Validation Methods Design Automation, Languages, and Simulations Plunkett's Engineering & Research Industry Almanac 2008 Logic Synthesis and Verification Co-verification of Hardware and Software for ARM SoC Design

Specification and design methodology has seen significant growth as a research area over the last decade, tracking but lagging behind VLSI design technology in general and the CAD industry in particular. The commercial rush to market tries to leverage existing technology which fuels CAD design tool development. Paralleling this is very active basic and applied research to investigate and move forward rational and effective methodologies for accomplishing digital design, especially in the field of hardware/software codesign. It is this close relationship between industry and academia that makes close cooperation between researchers and practitioners so important-and monographs like this that combine both abstract concept and pragmatic implementation deftly bridge this often gaping chasm. It was at the IEEE/ACM Eighth International Symposium on Hardware/Software Codesign where I met the author of this monograph, Dr. Randall Janka, who was presenting some of his recent dissertation research results on specification and design methodology, or as he has so succinctly defined this sometimes ambiguous concept, "the tools and rules." Where so many codesign researchers are trying to prove out different aspects of codesign and using toy applications to do so, Dr. Janka had developed a complete specification and design methodology and prototyped the infrastructure-and proven its viability, utility, and effectiveness using a demanding real-world application of a real-time synthetic aperture radar imaging processor that was implemented with embedded

parallel processors. This book presents a new methodology with reduced time impact to address the problem of analog integrated circuit (IC) yield estimation by means of Monte Carlo (MC) analysis, inside an optimization loop of a population-based algorithm. The low time impact on the overall optimization processes enables IC designers to perform yield optimization with the most accurate yield estimation method, MC simulations using foundry statistical device models considering local and global variations. The methodology described by the authors delivers on average a reduction of 89% in the total number of MC simulations, when compared to the exhaustive MC analysis over the full population. In addition to describing a newly developed yield estimation technique, the authors also provide detailed background on automatic analog IC sizing and optimization. This volume constitutes the refereed proceedings of the Third International Conference on Industrial Applications of Holonic and Multi-Agent Systems held in September 2007. The 39 full papers were selected from among 63 submissions. They are organized into topical sections covering theoretical and methodological issues, algorithms and technologies, implementation and validation, applications, and supply chain management. The first of two volumes in the Electronic Design Automation for Integrated Circuits Handbook, Second Edition, Electronic Design Automation for IC System Design, Verification, and Testing thoroughly examines system-level design, microarchitectural design, logic verification, and testing. Chapters contributed by leading experts authoritatively discuss processor modeling and design tools, using performance metrics to select microprocessor cores for integrated circuit (IC) designs, design and verification languages, digital simulation, hardware acceleration and emulation, and much more. New to This Edition: Major updates appearing

in the initial phases of the design flow, where the level of abstraction keeps rising to support more functionality with lower non-recurring engineering (NRE) costs Significant revisions reflected in the final phases of the design flow, where the complexity due to smaller and smaller geometries is compounded by the slow progress of shorter wavelength lithography New coverage of cutting-edge applications and approaches realized in the decade since publication of the previous edition—these are illustrated by new chapters on high-level synthesis, system-on-chip (SoC) block-based design, and back-annotating system-level models Offering improved depth and modernity, Electronic Design Automation for IC System Design, Verification, and Testing provides a valuable, state-of-the-art reference for electronic design automation (EDA) students, researchers, and professionals. Market research guide to the infotech industry a tool for strategic planning, competitive intelligence, employment searches or financial research. Contains trends, statistical tables, and an industry glossary. Includes one page profiles of infotech industry firms, which provides data such as addresses, phone numbers, executive names. This book describes new tools for front end analog designers, starting with global variation-aware sizing, and extending to novel variation-aware topology design. The tools aid design through automation, but more importantly, they also aid designer insight through automation. We now describe four design tasks, each more general than the previous, and how this book contributes design aids and insight aids to each. The ?rst designer task targeted is global robust sizing. This task is supported by a design tool that does automated, globally reliable, variation-aware s- ing (SANGRIA),and an insight-aiding tool that extracts designer-interpretable whitebox models that relate sizings to circuit performance (CAFFEINE). SANGRIA searches on several

levels of problem dif?culty simultaneously, from lower cheap-to-evaluate “exploration” layers to higher full-evaluation “exploitation” layers (structural homotopy). SANGRIAmakes maximal use of circuit simulations by performing scalable data mining on simulation results to choose new candidate designs. CAFFEINE accomplishes its task by tre- ing function induction as a tree-search problem. It constrains its tree search space via a canonical-functional-form grammar, and searches the space with grammatically constrained genetic programming. The second designer task is topology selection/topology design. Topology selection tools must consider a broad variety of topologies such that an app-priate topology is selected, must easily adapt to new semiconductor process nodes, and readily incorporate new topologies. Topology design tools must allow designers to creatively explore new topology ideas as rapidly as possible. Digital VLSI Chip Design with Cadence and Synopsys CAD Tools leads students through the complete process of building a ready-to-fabricate CMOS integrated circuit using popular commercial design software. Detailed tutorials include step-by-step instructions and screen shots of tool windows and dialog boxes. This hands-on book is for use in conjunction with a primary textbook on digital VLSI. University instructors may order Digital VLSI Chip Design with Cadence and Synopsys CAD Tools with the following textbooks: [Rabaey Cover Image] Digital Integrated Circuits, 2nd Edition, by Jan M. Rabaey, Anantha Chandrakasan, and Borivoje Nikoli. To order Digital Integrated Circuits, 2nd Edition packaged with Digital VLSI Chip Design with Cadence and Synopsys CAD Tools, please use ISBN 0-13-509470-4 on your bookstore order form. [Weste Cover Image] CMOS VLSI Design, 3rd Edition, by Neil H.E. Weste and David Harris. To order CMOS VLSI Design, 3rd Edition packaged with Digital VLSI Chip Design with Cadence and Synopsys CAD Tools, please use ISBN 0-13-509469-0 on your

bookstore order form. For further details, please contact your local Pearson (Addison-Wesley and Prentice Hall) sales representative or visit www.pearsonhighered.com. The Verilog Hardware Description Language (Verilog-HDL) has long been the most popular language for describing complex digital hardware. It started life as a prop- etary language but was donated by Cadence Design Systems to the design community to serve as the basis of an open standard. That standard was formalized in 1995 by the IEEE in standard 1364-1995. About that same time a group named Analog Verilog International formed with the intent of proposing extensions to Verilog to support analog and mixed-signal simulation. The first fruits of the labor of that group became available in 1996 when the language definition of Verilog-A was released. Verilog-A was not intended to work directly with Verilog-HDL. Rather it was a language with Similar syntax and related semantics that was intended to model analog systems and be compatible with SPICE-class circuit simulation engines. The first implementation of Verilog-A soon followed: a version from Cadence that ran on their Spectre circuit simulator. As more implementations of Verilog-A became available, the group defining the a- log and mixed-signal extensions to Verilog continued their work, releasing the defi- tion of Verilog-AMS in 2000. Verilog-AMS combines both Verilog-HDL and Verilog-A, and adds additional mixed-signal constructs, providing a hardware description language suitable for analog, digital, and mixed-signal systems. Again, Cadence was first to release an implementation of this new language, in a product named AMS Designer that combines their Verilog and Spectre simulation engines. As the complexity of electronic systems continues to increase, the micro-electronic industry depends upon automation and simulations to adapt quickly to market changes and new technologies. Compiled from chapters contributed to

CRC's best-selling VLSI Handbook, this volume of the Principles and Applications in Engineering series covers a broad rang This book provides comprehensive coverage of verification and debugging techniques for embedded software, which is frequently used in safety critical applications (e.g., automotive), where failures are unacceptable. Since the verification of complex systems needs to encompass the verification of both hardware and embedded software modules, this book focuses on verification and debugging approaches for embedded software with hardware dependencies. Coverage includes the entire flow of design, verification and debugging of embedded software and all key approaches to debugging, dynamic, static, and hybrid verification. This book discusses the current, industrial embedded software verification flow, as well as emerging trends with focus on formal and hybrid verification and debugging approaches. A guide to the trends and leading companies in the engineering, research, design, innovation and development business fields: those firms that are dominant in engineering-based design and development, as well leaders in technology-based research and development. This material, which includes a full-colour textbook and over 12 hours of video tutorials (in mp4 format), provides a comprehensive guide for the RF and Microwave engineering student or junior professional. It allows the reader to achieve a good understanding of the foundation theory and concepts behind high frequency circuits as well illustrating the most common design and simulation techniques for passive and active RF circuits. This state-of-the-art survey gives a systematic presentation of recent advances in the design and validation of computer architectures. The book covers a comprehensive range of architecture design and validation methods, from computer aided high-level design of VLSI circuits and systems to layout and testable design, including the modeling and synthesis of

behavior and dataflow, cell-based logic optimization, machine assisted verification, and virtual machine design. This useful book addresses electrothermal problems in modern VLSI systems. It discusses electrothermal phenomena and the fundamental building blocks that electrothermal simulation requires. The authors present three important applications of VLSI electrothermal analysis: temperature-dependent electromigration diagnosis, cell-level thermal placement, and temperature-driven power and timing analysis. Complete PCB Design Using OrCAD Capture and PCB Editor, Second Edition, provides practical instruction on how to use the OrCAD design suite to design and manufacture printed circuit boards. Chapters cover how to Design a PCB using OrCAD Capture and OrCAD Layout, adding PSpice simulation capabilities to a design, how to develop custom schematic parts, how to create footprints and PSpice models, and how to perform documentation, simulation and board fabrication from the same schematic design. This book is suitable for both beginners and experienced designers, providing basic principles and the program's full capabilities for optimizing designs. Presents a fully updated edition on OrCAD Capture, Version 17.2 Combines the theoretical and practical parts of PCB design Includes real-life design examples that show how and why designs work, providing a comprehensive toolset for understanding OrCAD software Provides the exact order in which a circuit and PCB are designed Introduces the IPC, JEDEC and IEEE standards relating to PCB design Modern telecommunication systems are highly complex from an algorithmic point of view. The complexity continues to increase due to advanced modulation schemes, multiple protocols and standards, as well as additional functionality such as personal organizers or navigation aids. To have short and reliable design cycles, efficient verification methods and tools are necessary. Modeling and simulation need to

accompany the design steps from the specification to the overall system verification in order to bridge the gaps between system specification, system simulation, and circuit level simulation. Very high carrier frequencies together with long observation periods result in extremely large computation times and requires, therefore, specialized modeling methods and simulation tools on all design levels. The focus of Modeling and Simulation for RF System Design lies on RF specific modeling and simulation methods and the consideration of system and circuit level descriptions. It contains application-oriented training material for RF designers which combines the presentation of a mixed-signal design flow, an introduction into the powerful standardized hardware description languages VHDL-AMS and Verilog-A, and the application of commercially available simulators. Modeling and Simulation for RF System Design is addressed to graduate students and industrial professionals who are engaged in communication system design and want to gain insight into the system structure by own simulation experiences. The authors are experts in design, modeling and simulation of communication systems engaged at the Nokia Research Center (Bochum, Germany) and the Fraunhofer Institute for Integrated Circuits, Branch Lab Design Automation (Dresden, Germany). A complete guide to trends and leading companies in the Engineering and Research business fields, design, development and technology-based research. Includes market analysis, R&D data and several statistical tables. Nearly 400 in-depth profiles of Engineering and Research firms. This reference book is a complete guide to the trends and leading companies in the engineering, research, design, innovation and development business fields: those firms that are dominant in engineering-based design and development, as well leaders in technology-based research and development. We have included companies that are making

significant investments in research and development via as many disciplines as possible, whether that research is being funded by internal investment, by fees received from clients or by fees collected from government agencies. In this carefully-researched volume, you'll get all of the data you need on the American Engineering & Research Industry, including: engineering market analysis, complete industry basics, trends, research trends, patents, intellectual property, funding, research and development data, growth companies, investments, emerging technologies, CAD, CAE, CAM, and more. The book also contains major statistical tables covering everything from total U.S. R&D expenditures to the total number of scientists working in various disciplines, to amount of U.S. government grants for research. In addition, you'll get expertly written profiles of nearly 400 top Engineering and Research firms - the largest, most successful corporations in all facets of Engineering and Research, all cross-indexed by location, size and type of business. These corporate profiles include contact names, addresses, Internet addresses, fax numbers, toll-free numbers, plus growth and hiring plans, finances, research, marketing, technology, acquisitions and much more. This book will put the entire Engineering and Research industry in your hands. Purchasers of either the book or PDF version can receive a free copy of the company profiles database on CD-ROM, enabling key word search and export of key information, addresses, phone numbers and executive names with titles for every company profiled. This valuable and accessible work provides comprehensive information on America's top public companies, listing over 10,000 publicly traded companies from the New York, NASDAQ and OTC exchanges. All companies have assets of more than $5 million and are filed with the SEC. Each entry describes business activity, 5 year sales, income, earnings per share, assets and liabilities. Senior

employees, major shareholders and directors are also named. The seven indices give an unrivalled access to the information. Plunkett's InfoTech Industry Almanac presents a complete analysis of the technology business, including the convergence of hardware, software, entertainment and telecommunications. This market research tool includes our analysis of the major trends affecting the industry, from the rebound of the global PC and server market, to consumer and enterprise software, to super computers, open systems such as Linux, web services and network equipment. In addition, we provide major statistical tables covering the industry, from computer sector revenues to broadband subscribers to semiconductor industry production. No other source provides this book's easy-to-understand comparisons of growth, expenditures, technologies, imports/exports, corporations, research and other vital subjects. The corporate profile section provides in-depth, one-page profiles on each of the top 500 InfoTech companies. We have used our massive databases to provide you with unique, objective analysis of the largest and most exciting companies in: Computer Hardware, Computer Software, Internet Services, E-Commerce, Networking, Semiconductors, Memory, Storage, Information Management and Data Processing. We've been working harder than ever to gather data on all the latest trends in information technology. Our research effort includes an exhaustive study of new technologies and discussions with experts at dozens of innovative tech companies. Purchasers of the printed book or PDF version may receive a free CD-ROM database of the corporate profiles, enabling export of vital corporate data for mail merge and other uses.
The second of two volumes in the Electronic Design Automation for Integrated Circuits Handbook, Second Edition, Electronic Design Automation for IC Implementation, Circuit Design, and Process Technology thoroughly examines real-time logic (RTL) to GDSII (a

file format used to transfer data of semiconductor physical layout) design flow, analog/mixed signal design, physical verification, and technology computer-aided design (TCAD). Chapters contributed by leading experts authoritatively discuss design for manufacturability (DFM) at the nanoscale, power supply network design and analysis, design modeling, and much more. New to This Edition: Major updates appearing in the initial phases of the design flow, where the level of abstraction keeps rising to support more functionality with lower non-recurring engineering (NRE) costs Significant revisions reflected in the final phases of the design flow, where the complexity due to smaller and smaller geometries is compounded by the slow progress of shorter wavelength lithography New coverage of cutting-edge applications and approaches realized in the decade since publication of the previous edition—these are illustrated by new chapters on 3D circuit integration and clock design Offering improved depth and modernity, Electronic Design Automation for IC Implementation, Circuit Design, and Process Technology provides a valuable, state-of-the-art reference for electronic design automation (EDA) students, researchers, and professionals. Research and development of logic synthesis and verification have matured considerably over the past two decades. Many commercial products are available, and they have been critical in harnessing advances in fabrication technology to produce today's plethora of electronic components. While this maturity is assuring, the advances in fabrication continue to seemingly present unwieldy challenges. Logic Synthesis and Verification provides a state-of-the-art view of logic synthesis and verification. It consists of fifteen chapters, each focusing on a distinct aspect. Each chapter presents key developments, outlines future challenges, and lists essential references. Two unique features of this book are technical strength and

comprehensiveness. The book chapters are written by twenty-eight recognized leaders in the field and reviewed by equally qualified experts. The topics collectively span the field. Logic Synthesis and Verification fills a current gap in the existing CAD literature. Each chapter contains essential information to study a topic at a great depth, and to understand further developments in the field. The book is intended for seniors, graduate students, researchers, and developers of related Computer-Aided Design (CAD) tools. From the foreword: "The commercial success of logic synthesis and verification is due in large part to the ideas of many of the authors of this book. Their innovative work contributed to design automation tools that permanently changed the course of electronic design." by Aart J. de Geus, Chairman and CEO, Synopsys, Inc. The Accellera Universal Verification Methodology (UVM) standard is architected to scale, but verification is growing and in more than just the digital design dimension. It is growing in the SoC dimension to include low-power and mixed-signal and the system integration dimension to include multi-language support and acceleration. These items and others all contribute to the quality of the SOC so the Metric-Driven Verification (MDV) methodology is needed to unify it all into a coherent verification plan. This book is for verification engineers and managers familiar with the UVM and the benefits it brings to digital verification but who also need to tackle specialized tasks. It is also written for the SoC project manager that is tasked with building an efficient worldwide team. While the task continues to become more complex, Advanced Verification Topics describes methodologies outside of the Accellera UVM standard, but that build on it, to provide a way for SoC teams to stay productive and profitable. Multi-volume major reference work bringing together histories of companies that are a leading

influence in a particular industry or geographic location. For students, job candidates, business executives, historians and investors. The aim of the CEEMAS conference series is to provide a biennial forum for the presentation of multi-agent research and development results. With its p- ticular geographicalorientation towards Central and Eastern Europe, CEEMAS has become an internationally recognised event with participants from all over the world. After the successful CEEMAS conferences in St. Petersburg (1999), Cracow (2001) and Prague (2003), the 2005 CEEMAS conference takes place in Budapest. The programme committee of the conference series consists of est- lished researchers from the region and renowned international colleagues, sh- ing the prominent rank of CEEMAS among the leading events in multi-agent systems. In the very competitive ?eld of agent oriented conferences and workshops nowadays(suchasAAMAS,WI/IAT,EU MAS,CIA,MATES)thespecialpro?le of CEEMAS is that it is trying to bridge the gap between applied research achievements and theoretical research activities. Our ambition is to provide a forum for presenting theoretical research with an evident application potential, implemented application prototypes and their properties, as well as industrial case studies of successful (but also unsuccessful) agent technology deployments. This is why the CEEMAS proceedings volume provides a collection of research and application papers. The technical research paper section of the proceedings (see pages 11–499) contains pure research papers as well as research results in application settings while the application papers section (see pages 500–530) contains papers focused on application aspects. The goal is to demonstrate the real life value and commercial reality of multi-agent systems as well as to foster communication between academia and industry in this ?eld. The Complete, Modern Tutorial on Practical

VLSI Chip Design, Validation, and Analysis As microelectronics engineers design complex chips using existing circuit libraries, they must ensure correct logical, physical, and electrical properties, and prepare for reliable foundry fabrication. VLSI Design Methodology Development focuses on the design and analysis steps needed to perform these tasks and successfully complete a modern chip design. Microprocessor design authority Tom Dillinger carefully introduces core concepts, and then guides engineers through modeling, functional design validation, design implementation, electrical analysis, and release to manufacturing. Writing from the engineer’s perspective, he covers underlying EDA tool algorithms, flows, criteria for assessing project status, and key tradeoffs and interdependencies. This fresh and accessible tutorial will be valuable to all VLSI system designers, senior undergraduate or graduate students of microelectronics design, and companies offering internal courses for engineers at all levels. Reflect complexity, cost, resources, and schedules in planning a chip design project Perform hierarchical design decomposition, floorplanning, and physical integration, addressing DFT, DFM, and DFY requirements Model functionality and behavior, validate designs, and verify formal equivalency Apply EDA tools for logic synthesis, placement, and routing Analyze timing, noise, power, and electrical issues Prepare for manufacturing release and bring-up, from mastering ECOs to qualification This guide is for all VLSI system designers, senior undergraduate or graduate students of microelectronics design, and companies offering internal courses for engineers at all levels. It is applicable to engineering teams undertaking new projects and migrating existing designs to new technologies. Formal Verification: An Essential Toolkit for Modern VLSI Design presents practical approaches for design and validation, with

hands-on advice to help working engineers integrate these techniques into their work. Formal Verification (FV) enables a designer to directly analyze and mathematically explore the quality or other aspects of a Register Transfer Level (RTL) design without using simulations. This can reduce time spent validating designs and more quickly reach a final design for manufacturing. Building on a basic knowledge of SystemVerilog, this book demystifies FV and presents the practical applications that are bringing it into mainstream design and validation processes at Intel and other companies. After reading this book, readers will be prepared to introduce FV in their organization and effectively deploy FV techniques to increase design and validation productivity. Learn formal verification algorithms to gain full coverage without exhaustive simulation Understand formal verification tools and how they differ from simulation tools Create instant test benches to gain insight into how models work and find initial bugs Learn from Intel insiders sharing their hard-won knowledge and solutions to complex design problems UNISCON 2009 (United Information Systems Conference) was the third conf- ence in the series that is based on the idea to pool smaller but highly interesting scienti?c events on information systems into one large conference. Here, people from di?erent scienti?c backgrounds can present their research results, share their ideas and discuss future trends in these various areas. UNISCON 2009 was held in Sydney, Australia in the University of Western Sydney, Campbelltown Campus. In 2009 the following scienti?c events were held under the umbrella of UNISCON 2009: th – 8 International Conference on Information Systems Technology and Its Applications (ISTA 2009) th – 8 International Workshop on Conceptual Modelling Approaches for e- Business (eCOMO 2009) – Second Workshop on Model-Based Software and Data Integration

(MBSDI 2009) We received 115 papers for the three events. Papers were submitted from over 25 countries. After a rigorous review process, 39 papers were accepted as full papers and 14 papers as short papers for presentation at the conference and published in these proceedings. In addition to the above three events, we also organized a Doctoral Cons- tium to provide a forum for doctoral students to get feedback from experts in the area about their research projects. This book, the Mixed-signal Methodology Guide: Advanced Methodology for AMS IP and SoC Design, Verification, and Implementation provides a broad overview of the design, verification and implementation methodologies required for today's mixed-signal designs. The book covers mixed-signal design trends and challenges, abstraction of analog using behavioral models, assertion-based metric-driven verification methodology applied on analog and mixed-signal and verification of low power intent in mixed-signal design. It also describes methodology for physical implementation in context of concurrent mixed-signal design and for handling advanced node physical effects. The book contains many practical examples of models and techniques. The authors believe it should serve as a reference to many analog, digital and mixed-signal designers, verification, physical implementation engineers and managers in their pursuit of information for a better methodology required to address the challenges of modern mixed-signal design. Market research guide to the infotech industry a tool for strategic planning, competitive intelligence, employment searches or financial research. Contains trends, statistical tables, and an industry glossary. Includes one page profiles of infotech industry firms, which provides data such as addresses, phone numbers, and executive names. Hardware/software co-verification is how to make sure that embedded system software works correctly with the hardware, and that the hardware has

been properly designed to run the software successfully -before large sums are spent on prototypes or manufacturing. This is the first book to apply this verification technique to the rapidly growing field of embedded systems-on-a-chip(SoC). As traditional embedded system design evolves into single-chip design, embedded engineers must be armed with the necessary information to make educated decisions about which tools and methodology to deploy. SoC verification requires a mix of expertise from the disciplines of microprocessor and computer architecture, logic design and simulation, and C and Assembly language embedded software. Until now, the relevant information on how it all fits together has not been available. Andrews, a recognized expert, provides in-depth information about how co-verification really works, how to be successful using it, and pitfalls to avoid. He illustrates these concepts using concrete examples with the ARM core - a technology that has the dominant market share in embedded system product design. The companion CD-ROM contains all source code used in the design examples, a searchable e-book version, and useful design tools. * The only book on verification for systems-on-a-chip (SoC) on the market * Will save engineers and their companies time and money by showing them how to speed up the testing process, while still avoiding costly mistakes * Design examples use the ARM core, the dominant technology in SoC, and all the source code is included on the accompanying CD-Rom, so engineers can easily use it in their own designs This book covers issues and solutions in the physical integration and tapeout management for VLSI design. Chapter 1 gives the overview. Chapter 2 shows detailed techniques for physical design. Chapter 3 provides CAD flows. Chapter 4 discusses on-chip interconnects. A glossary of keywords is provided at the end. Plunkett's InfoTech Industry Almanac presents a complete analysis of the technology business, including the convergence of

hardware, software, entertainment and telecommunications. This market research tool includes our analysis of the major trends affecting the industry, from the rebound of the global PC and server market, to consumer and enterprise software, to super computers, open systems such as Linux, web services and network equipment. In addition, we provide major statistical tables covering the industry, from computer sector revenues to broadband subscribers to semiconductor industry production. No other source provides this book's easy-to-understand comparisons of growth, expenditures, technologies, imports/exports, corporations, research and other vital subjects. The corporate profile section provides in-depth, one-page profiles on each of the top 500 InfoTech companies. We have used our massive databases to provide you with unique, objective analysis of the largest and most exciting companies in: Computer Hardware, Computer Software, Internet Services, E-Commerce, Networking, Semiconductors, Memory, Storage, Information Management and Data Processing. We've been working harder than ever to gather data on all the latest trends in information technology. Our research effort includes an exhaustive study of new technologies and discussions with experts at dozens of innovative tech companies. Purchasers of the printed book or PDF version may receive a free CD-ROM database of the corporate profiles, enabling export of vital corporate data for mail merge and other uses. Presenting a comprehensive overview of the design automation algorithms, tools, and methodologies used to design integrated circuits, the Electronic Design Automation for Integrated Circuits Handbook is available in two volumes. The first volume, EDA for IC System Design, Verification, and Testing, thoroughly examines system-level design, microarchitectural design, logical verification, and testing. Chapters contributed by leading experts authoritatively discuss processor

modeling and design tools, using performance metrics to select microprocessor cores for IC designs, design and verification languages, digital simulation, hardware acceleration and emulation, and much more. Save on the complete set.

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- Variation Aware Analog Structural Synthesis
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- Complete PCB Design Using OrCAD Capture And PCB Editor
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- Multi Agent Systems And Applications IV
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